

### **REMARKS**

This response is intended as a complete response to the Office Action dated October 16, 2009. In view of the following discussion, the Applicants believe that all claims are in allowable form.

### **CLAIM REJECTIONS**

#### **1. 35 USC §103 Claims 1, 3-18, and 36-53**

Claims 1-18 and 36-53 stand rejected under 35 USC §103 as being unpatentable over US Patent No. 6,625,497, issued September 23, 2003, to *Fairbairn, et al.* (hereinafter *Fairbairn*) in view of US Patent Application Publication No. 2004/0078108, published April 22, 2004, to *Choo, et al.* (hereinafter *Choo*) and further in view of US Patent 6,567,717, issued May 20, 2003, to *Krivokapic, et al.* (hereinafter *Krivokapic*) and US Patent Application No. 2004/0087041 published May 6, 2004 to *Perry, et al.* (hereinafter *Perry*).

The Applicants respectfully disagree for the reasons discussed below. However, in response to the Office Action dated 10/16/09, the Applicants have amended claims 1 and 36 to clarify the limitations recited in the claims. The Applicants submit that the amendments to the independent claims 1 and 36 are not made in view of the cited art and further submit that the amended claims do not further limit the scope of the claims. Rather, these amendments merely make more clear that which was already recited in the claims. As such, the Applicants further submit that these amendments add no new matter.

The Applicants have amended claim 1 to recite, in relevant part, executing a multi-pass process wherein the substrate is processed more than once by a pass, wherein each pass includes a measurement process, an etch process, and at least one post-etch process while forming the at least one structure. The Applicants have similarly amended claim 36 to recite, in relevant part, executing a multi-pass process, wherein the substrate is processed more than once by a pass, wherein each pass includes at least one measurement process, an etch process and at least one pre-etch process and/or at least one post-etch process while forming at least one structure on the substrate.

The teachings of the cited art have been discussed extensively in prior Office Action Responses. As relevant here, the Examiner contends in the Office Action dated 10/16/09 that the combination of the cited art results in a method, wherein an etch process is performed in an etch reactor and wherein an at least one post-etch process is performed in substrate processing equipment external to the etch reactor, or wherein the etch process is performed in an etch reactor and the at least one pre-etch process and the at least one post-etch process is performed in substrate processing equipment external to the etch reactor.

Specifically, in the Response to Arguments of the present Office Action dated 10/16/09, the Examiner argues that *Fairbairn* allegedly discloses a post-etch process performed in substrate processing equipment external to the etch reactor. (*Office Action dated 10/16/09*, p. 18.) The Examiner contends that a post-etch critical dimension (CD) measurement as taught by *Fairbairn* reads on a post-etch process performed in substrate processing equipment external to the etch reactor. (*Id.*, p.4; citing *Fairbairn*, col. 12, ll. 34-45 and ll. 53-63.) The Applicants respectfully disagree.

The Applicants respectfully submit that a post-etch CD measurement as taught by *Fairbairn* fails to read on a post-etch process performed in substrate processing equipment external to the etch reactor, as recited in independent claims 1 and 36.

Independent claim 1 recites adjusting a process recipe of at least one post-etch process using the results of measuring the dimensions on the structures. Similarly, independent claim 36 recites adjusting a process recipe of at least one pre-etch process and/or at least one post etch process using the results of measuring the dimensions on the structures. Accordingly, if one substitutes "post-etch process" with "post-etch CD measurement" in the independent claims 1 and 36, as would result if the Examiner's contention were followed, the claims would read, "adjusting a process recipe of a post-etch CD measurement using the results of measuring the dimensions on the structures." Clearly, the Examiner will appreciate that this statement makes no sense as it calls for adjusting the process recipe of a measurement process using the results of the measurement process. Furthermore, even if such a process were possible, *Fairbairn* fails to teach or suggest adjusting

the process recipe of a CD measurement using the results of measuring the dimensions on structures. To the contrary, *Fairbairn* teaches the process recipe of a process to be performed on a wafer, such as an etch process, is selected based on a CD measurement. (*Fairbairn*, Abstract.) Accordingly, a post-etch CD measurement, or any CD measurement of *Fairbairn* fails to read on the post-etch process as recited in the claims.

Further, the Examiner contends photoresist trimming or shrinking read on a pre-etch process performed in substrate processing equipment external to the etch reactor as recited in claim 36. (*Office Action dated 10/16/09*, p. 4; citing *Fairbairn*, col. 13, line 44.) However, the Applicants note that *Fairbairn* teaches that the photoresist trimming is performed in the etcher 902. (*Fairbairn*, col. 13, ll. 41-44.) Accordingly, *Fairbairn* further fails to teach or suggest a pre-etch process performed in substrate processing equipment external to the etch reactor as recited in claim 36.

The Examiner admits that the combination of *Fairbairn* and *Choo* fails to teach a multi-pass process. *Krivokapic* is cited for the proposition that it teaches that, after a post-etch measurement, wafers may be returned for further etching if under-etched. (*Office Action dated 10/16/09*, p. 6; citing *Krivokapic*, col. 10, line 35.) However, even if *Krivokapic* teaches to return to the substrate to an etch reactor for a second time further etching if under-etched, the combination of cited art fails to teach, suggest or otherwise yield a multi-pass process as recited in independent claims 1 and 36.

*Krivokapic* teaches that after a post-etch measurement, wafers may be returned for further etching if under-etched. The return of an under-etched wafer to the etcher of *Krivokapic* for rework is a return to the same etcher. However, *Krivokapic* teaches only to measure a wafer and return the wafer to the etcher for re-etching, and fails to teach, suggest, or otherwise yield, performing a multi-pass process including a measurement process, an etch process, and at least one post-etch process while forming the at least one structure.

*Krivokapic* is silent regarding a pre-etch process or a post-etch process performed in substrate processing equipment external to the etch reactor as recited in the independent claims, and is further silent regarding each pass of a multi-pass

process, wherein a pass includes a measurement process, an etch process, and a post-etch process (claim 1) or at least one of a pre-etch or post-etch process (claim 36).

Accordingly, even if *Krivokapic* teaches to etch the wafer more than once using an etching process, *Krivokapic* fails to teach, suggest, or otherwise yield a multi-pass process wherein the substrate is processed more than once by a pass, wherein each pass includes a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, as recited in claim 1; or a multi-pass process, wherein the substrate is processed more than once by a pass, wherein each pass includes at least one measurement process, an etch process and at least one pre-etch process and/or at least one post-etch process while forming at least one structure on the substrate as recited in claim 36.

In the Response to Arguments section of the Office Action dated 10/16/09, the Examiner further contends that *Fairbairn* allegedly teaches post-etch processing, such as ash stripping, wet cleaning and/or further CD measurement before the wafer is returned to the cassette. (*Office Action dated 10/16/09*, p. 18; citing *Fairbairn*, Abstract.) Further, the Examiner contends that it would be obvious to perform a process, such as cleaning and/or CD measurement at least one more time to insure that the multi-pass process was successful. (*Id.*, p. 19.) The Applicants respectfully disagree that the Examiners hypothetical process would meet the limitations explicitly recited in the claims.

As discussed above, the CD measurement and the photoresist trimming processes of *Fairbairn* fail to read on a post-etch process or a pre-etch process as recited in the claims.

Regarding processes, such as ash stripping or cleaning, *Fairbairn* teaches after etching a wafer at step 1060, the wafer may returned to the cassette 908; or alternatively, transferred to measurement tool 906 for a post-etch CD measurement prior to returning to the cassette 908; or alternatively, ashed in an ash strip processor (ASP) 909 to remove photoresist polymers and other residue from wafers after etching and then transferred to the measurement tool 906 for post-etch CD measurement prior to returning to the cassette 908; or alternatively, ashed in the

ASP 909 and cleaned in a cleaning module 911 prior to post-etch CD measurement and return to the cassette 908. (*Fairbairn*, col. 12, ll. 16-63; Figures 9A-C, 10.)

Specifically, *Fairbairn* teaches that after etching, ash stripping or wet cleaning is utilized to remove photoresist polymers and other residues. (*Id.*, col. 12, ll. 37-38.) Accordingly, it would not be obvious to repeat a second pass of a multi-pass process, wherein the second pass included a measurement process, an etch process, and a post-etch process, because after etching the wafer on a first pass, *Fairbairn* teaches to remove the photoresist by ash stripping or wet cleaning. Thus, once the photoresist has been removed, the wafer would not be returned for further etching during a second pass in the manner suggested by the Examiner.

*Perry* is cited to show a control etch method based on an *in-situ* thickness measurement step. However, *Perry* fails to teach or suggest executing a multi-pass process wherein the substrate is processed more than once by a pass, wherein each pass includes a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, as recited in claim 1, or executing a multi-pass process, wherein the substrate is processed more than once by a pass, wherein a pass includes at least one measurement process, an etch process and at least one pre-etch process and/or at least one post-etch process while forming at least one structure on the substrate; and measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on the substrate, during each at least one measurement process, as recited in claim 36. Hence, *Perry* fails to teach or suggest a modification of *Fairbairn*, *Choo*, and *Krivokapic* of that would yield the limitations recited in claims 1 and 36. Therefore, a *prima facie* case of obviousness has not been established as the combination of the cited references fails to yield the limitations recited in the claims.

Thus, the Applicants submit that independent claims 1 and 36, and claims 3-18 and 37-52, respectively depending therefrom, are patentable over *Fairbairn* in view of *Choo*, and further in view of *Krivokapic* and *Perry*. Accordingly, the Applicants respectfully request that the rejection be withdrawn and the claims allowed.

2. 35 USC §103 Claims 19-21

Claims 19-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Fairbairn* in view of *Choo*, *Krivokapic*, and *Perry*, as applied above to claim 1, and further in view of US Patent Application No. 2003/0022510 published January 30, 2003 to *Morgenstern* (hereinafter *Morgenstern*).

Independent claim 1, from which claims 19-21 depend, recites limitations not taught or suggested by any permissible combination of the cited art. The patentability of claim 1 over the combination of *Fairbairn*, *Choo*, *Krivokapic*, and *Perry*, is discussed above.

The Examiner cites *Morgenstern* to show a process of forming a capacitive trench structure with a polysilicon electrode layer wherein the etch process is performed with an HBr and Cl<sub>2</sub> chemistry. (*Office Action dated 10/16/09*, p. 17, citing *Morgenstern*, ¶¶ [0033-0034, 0044].) Even if *Morgenstern* teaches forming a capacitive trench structure, *Morgenstern* still fails to teach or suggest executing a multi-pass process wherein the substrate is processed more than once by a pass, wherein each pass includes a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, wherein the etch process is performed in an etch reactor and wherein the at least one post-etch process is performed in substrate processing equipment external to the etch reactor, as recited in claim 1.

Hence, *Morgenstern* fails to teach or suggest a modification of *Fairbairn* in view of *Choo*, *Krivokapic*, and *Perry* that would yield the limitations recited in claim 1. Therefore, a *prima facie* case of obviousness has not been established as the combination of the cited references fails to yield the limitations recited in the claims.

Thus, the Appellants submit that claims 19-21 are patentable over *Fairbairn* in view of *Choo*, *Krivokapic*, and *Perry* and further in view of *Morgenstern*. Accordingly, the Appellants respectfully request that the rejection be withdrawn and the claims allowed.

**NEW CLAIMS**

The Applicants have added a new claims 54-55. New claims 54-55 respectively depend from claims 1 and 36 and are patentable over the cited art for at least the reasons discussed above. Moreover, new claims 54-55 each recite etching a first layer during a first pass of the multi-pass process; depositing a second layer atop the etched first layer; and etching the second layer during a second pass of the multi-pass process. The Applicants submit that, for similar reasons as discussed above, such limitations are not taught or suggested by *Krivokapic* (as relied upon by the Examiner to establish a multi-pass process), nor by any other combination of the cited art.

The Applicants submit that no new matter has been added, and respectfully request that the additional claim be entered and allowed.

**CONCLUSION**

Thus, the Applicants believe that all claims now pending are presently in condition for allowance. Accordingly, both further consideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Alan Taboada at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

January 18, 2010

/ Alan Taboada /  
Alan Taboada, Esq.  
Reg. No. 51,359  
(732) 935-7100

Moser IP Law Group  
1030 Broad Street, 2<sup>nd</sup> Floor  
Shrewsbury, NJ 07702